REMARKS

Favorable reconsideration and allowance of the present application are respectfully requested in view of the following remarks. Claims 1-4 and 6-17 were pending prior to the Office Action. Claims 19-23 have been added. Therefore, claims 1-4 and 6-23 are pending. Claims 1, 6, 10 and 19 are independent.

§ 112, 2ND PARAGRAPH REJECTION

Claims 10-18 stand rejected under 35 USC 112, second paragraph, as allegedly being indefinite. *See Office Action, page 2, items 3 and 4*. Claim 10 has been amended as suggested in the Office Action. Applicant respectfully requests that the Section 112, second paragraph rejection of claims 10-18 be withdrawn.

§ 103 REJECTION - NOZUYAMA, NAKAJIMA, KELLEY

Claims 1, 6, and 10-18 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Nozuyama (USP 5,862,359) in view of Nakajima et al. (JP2000020459, hereinafter "Nakajima") and Kelley et al. (USP 6,134,621, hereinafter "Kelley"). Applicant traverses.

For a Section 103 rejection to be proper, a *prima facie* case of obviousness must be established. *See M.P.E.P. 2142.* One requirement to establish *prima facie case* of obviousness is that there must be a suggestion or motivation within the cited references to modify the references as proposed in the Office Action. *See M.P.E.P. 2143.01.* The cited reference must be considered in its entirety including disclosures that teach away from the claimed invention. *See M.P.E.P. 2141.02.* If the cited references teach away from the claimed invention, then the combination is improper and the rejection must fail.

In this instance, Nozuyama teaches away from Nakajima as well as away from the claimed invention. More specifically, Nozuyama is directed toward a data transfer bus provided between a plurality of functional blocks inside a large scale integrated circuit (LSI) or a very large scale integrated circuit (VLSI) or between a plurality of LSI's. The primary objective of Nozuyama is to provide low power consumption data transfer bus such as a bus that is used in a micro-processor, a micro-controller or the like. *See column 1, lines 7-14.*

Nozuyama discloses that Figure 1 is an example circuit diagram showing a low power consumption data transfer bus of an LSI. In Figure 1, the LSI can include a plurality of function

blocks 11-16, a bus switch circuit 3, and a decoder 4. It is shown that function blocks 11-16 are pair-wise divided and connected to three divisional buses 21, 22, and 23. More specifically, the function blocks 11 and 12 are connected divisional bus 21, function blocks 13 and 14 are connected to the divisional bus 22 and blocks 15 and 16 are connected to the divisional bus 23. *See Figure 1; column 3, lines 10-35.*

As mentioned above, Nozuyama describes a procedure for a division of the buses and the connections of the functional blocks thereon are primarily driven to achieve low power consumption. *See column 4, lines 4-6.* Nozuyama discloses that a pair of functional blocks which have the highest average access frequency, for example functional blocks 11 and 12 are connected to one of the divisional buses, for example the divisional bus 21, which has the smallest load. *See Figure 1; column 3, lines 29-35.* In other words, if a pair of functional blocks such as a CPU and a related memory, they are connected to a common divisional bus. This is logical assuming that the CPU accesses the related memory very frequently.

Nozuyama also discloses the following. There may be a situation in which it must be decided whether another pair of functional blocks is connected to the same divisional bus as the

first pair of functional blocks or to another divisional bus. Nozuyama discloses that if the functional blocks are substantially independent from each other, the second pair of functional blocks should be connected to a different divisional bus. *See column 4, lines 13-22*. Referring back to Fig. 1, if the functional blocks 13 and 14 are substantially independent of functional blocks 11 and 12, then it would be logical to connect the functional blocks 13 and 14 to divisional bus 22 rather than to divisional bus 21.

A situation of independence might come as a result of the following. The LSI device 10 may include multiple CPU's and multiple memories with each memory dedicated for a particular CPU. For example, the function block 13 may be a second CPU in the device 10 and the function block 14 may be a second memory primarily dedicated to the access by the CPU 13. Presumably, the function blocks 13 and 14 is substantially independent of the function blocks 11 and 12 and thus do not always need to communicate with each other. If and when the communication is needed, the communication may take place via the bus switch 3.

Clearly, in this example, there is no guarantee of any speed differential between the pairwise function blocks 11 and 12 to that of pairwise function blocks 13 and 14.

In contrast, the Examiner asserts that Nakajima discloses a plurality of devices configured for high speed access and low speed access. *See Office Action, page 3, lines 20-23.* The Examiner also asserts that Nakajima discloses turning off the bus connection between the devices of the high speed access and the low speed access when the data is transferred to the device for high speed access. Thus, as asserted by the Examiner, Nakajima requires separation of devices between switches based on their access speeds. Even assuming the Examiner's assertions are taken to be true, this is in clear contrast to the teachings of Nozuyama which require no such division of speed differentials across the switches. Indeed, Nozuyama actually teaches away from Nakajima as asserted. Therefore, Nozuyama and Nakajima cannot be properly combined.

Further, combining Nozuyama with Nakajima would render each other's device unsatisfactory for its intended purpose. For example, modifying Nozuyama by the asserted teachings of Nakajima would not achieve the goal of minimizing power consumption of the LSI device. This clearly renders Nozuyama unsatisfactory for its intended purpose.

Kelley has not been, and indeed cannot be, relied upon to correct for at least the above noted deficiencies of Nozuyama

and Nakajima. Therefore, any rejection based on the combination of Nozuyama, Nakajima, and Kelley is improper.

Applicant respectfully requests that the rejection of claims 1, 6, and 10-18 based on Nozuyama, Nakajima and Kelley be withdrawn.

§ 103 REJECTION - NOZUYAMA, NAKAJIMA, KELLEY, CEPULIS

Claims 2-7 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Nozuyama, Nakajima, Kelley and Cepulis et al. (USP 6,061,754 hereinafter "Cepulis"). Applicant respectfully traverses.

It is noted that claims 2 and 7 depend from independent claims 1 and 6, respectively. It has also been shown that claims 1 and 6 are distinguishable over the combination of Nozuyama, Nakajima, and Kelley. Cepulis has not been, and indeed cannot be, relied upon to correct for at least the above noted deficiencies of Nozuyama, Nakajima and Kelley. Therefore, independent claims 1 and 6 are distinguishable over the combination of Nozuyama, Nakajima, Kelley and Cepulis. For at least due to the dependency thereon, dependent claims 2 and 7 are distinguishable over the combination of Nozuyama, Nakajima, Kelley and Cepulis.

Applicant respectfully requests that the rejection of claims 2 and 7 based on Nozuyama, Nakajima, Kelley and Cepulis be withdrawn.

§ 103 REJECTION - NOZUYAMA, NAKAJIMA, KELLEY, TSUKAMOTO

Claims 3, 4, 8 and 9 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Nozuyama, Nakajima, Kelley and Tsukamoto (USP 3,594,656). Applicant respectfully traverses.

It is noted that claims 3-4 and 8-9 depend from independent claims 1 and 6, respectively. It has also been shown that the independent claims are distinguishable over the combination of Nozuyama, Nakajima and Kelley. Tsukamoto has not been, and indeed cannot be, relied upon to correct for at least the above-noted deficiencies of Nozuyama, Nakajima and Kelley. Therefore, independent claims 1 and 6 are distinguishable over the combination of Nozuyama, Nakajima, Kelley and Tsukamoto.

For at least due to the dependency thereon, claims 3-4 and 8-9 are also distinguishable over the combination of Nozuyama, Nakajima, Kelley and Tsukamoto, as well as on their own merits.

Applicant respectfully requests that the rejection of claims 3-4 and 8-9 based on Nozuyama, Nakajima, Kelley and Tsukamoto be withdrawn.

NEW CLAIMS

By this reply, claims 19-23 have been added. All new claims are believed to be distinguishable over the cited references, individually or in any combination. Applicant respectfully requests that the new claims be allowed.

CONCLUSION

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance. Should there be any outstanding matters that need to be resolved, the Examiner is respectfully requested to contact Hyung Sohn (Reg. No. 44,346), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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